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Description

[METHOD FOR TREATING WAFER SURFACE]

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the priority benefit of Taiwan application serial no. 92104615, filed March 05, 2003.

BACKGROUND OF INVENTION

[0002] Field of Invention

[0003] The present invention relates to a method for treating a surface of a wafer. More particularly, the present invention relates to a method for removing residues on the surface of the wafer.

[0004] Description of Related Art

[0005] In the semiconductor industry, the manufacturing of integrated circuits (ICs) can be categorized as three stages: wafer production, IC fabrication and IC packaging. In general, the wafer is fabricated into chips through layout design, lithography/etching and wafer scribing. After com-

pleting the integrated circuits of the wafer, a plurality of bonding pads are formed on the active surface of the wafer and a passivation layer is formed to cover the active surface. The bonding pads exposed by the passivation layer are electrically connected to the external medium, for example, a package substrate or a circuit board. Taking the flip chip package as an example, after forming the bonding pads, bumps are formed on the wafer surface to electrically and mechanically connect the external package substrate or the circuit board. After the formation of bumps, the wafer is scribed into individual chip packages. Since bumps have high reliability and are arranged on the bonding pads in arrays, they are suitable to be applied in high-density flip chip packages, including flip chip/ball grid array packages.

[0006] Figs. 1A-1G are cross-sectional display views illustrating a conventional fabrication process for forming bumps. Referring to the Fig. 1A, a wafer 110 having an active surface 112 is provided. The wafer includes bonding pads 116 and a passivation layer 114 on the active surface 112. The bonding pads 116 are exposed through openings 118 of the passivation layer 114, so that the wafer can be electrically connected to the external circuit (not shown)

through the exposed bond pads.

[0007] Referring to Fig. 1B, a metal layer 130 is formed over the active surface 112 of the wafer 110, for enhancing adhesion. The metal layer 130 is a composite layer formed by either sputtering or evaporation. The material of the metal layer 130 includes titanium, tungsten, chromium, nickel, copper and the alloys thereof.

[0008] After forming the metal layer 130 on the active surface 112 of the wafer 110, a plurality of bumps are formed on the bonding pads 116 by either electroplating or screen printing.

[0009] Taking electroplating as an example, the following steps are described in Figs. 1C-1E.

[0010] As shown in Fig. 1C, a photoresist layer 140 is formed on the metal layer 130. After lithography and developing, the photoresist layer 140 is patterned to form a plurality of openings 142 therein, while openings 142 expose a portion of the metal layer 130.

[0011] Referring to Figs. 1D-1E, the openings 142 are filled by solder paste to form a plurality of solder (bump) paste globs 150 within the openings 142 by electroplating. The location of each solder paste glob 150 (opening) corresponds to the location of each bonding pad 116. After-

wards, the photoresist layer 140 is removed, leaving a portion of metal layer 130 between the solder paste globs 150 being exposed.

[0012] Referring to Figs. 1F-1G, using the solder paste globs as an etching mask, a wet etching process is performed to removed the exposed metal layer 130 between the solder paste globs 150, thus forming an under bump metallurgy (UBM) layer 132. Next, a reflow step is performed, so that the solder paste glob 150 becomes a globular bump 152.

[0013] However, as shown in Fig. 1E, if some photoresist 134 is not completely removed but remained on the metal layer 130 between the solder paste globs 150, the remained photoresist 134 will cause problems in the subsequent wet etching process. Because the remained photoresist 134 covers the underlying portion of the metal layer 130, the exposed metal layer 130 between the solder paste globs 150 can not be completely removed during the wet etching process and residual metal 136 stays on the passivation layer 114 between the globs 150. The residual metal can deteriorate the yield of the wafer. On the other hand, if the wet etching process is prolonged to remove the residual metal entirely, undercut of the UBM layer 132 may occur, which likewise decreases reliability for the

flip-chip packages. Therefore, it is important to remove residues of the UBM layer without degrading the UBM layer.

SUMMARY OF INVENTION

[0014] The present invention provides a method for treating the wafer surface, which can effectively remove residues on the wafer surface and increase the yield for the process.

[0015] As embodied and broadly described herein, the present invention provides a method for treating the wafer surface. A wafer having a plurality of bonding pads on its surface is provided. A plurality of bumps is formed on the bonding pads on the wafer surface, with one bump being attached to one bonding pad through the under bump metallurgy (UBM) layer. A photo-sensitive material layer is formed over the wafer surface, at least covering the UBM layer. Using the bumps as masks, the photo-sensitive material layer is patterned and developed to expose the wafer surface between the bumps. At least one wet etching process is performed to clean the exposed wafer surface, and the photo-sensitive material layer is removed.

[0016] It is to be understood that both the foregoing general description and the following detailed description are exemplary, and are intended to provide further explanation of

the invention as claimed.

Brief Description of Drawings

[0017] The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention.

[0018] Figs. 1A-1G are cross-sectional display views illustrating a conventional fabrication process for forming bumps.

[0019] Figs. 2A-2I are cross-sectional display views illustrating a method of treating the wafer surface according to one preferred embodiment of this invention.

Detailed Description

[0020] Figs. 2A-2I are cross-sectional display views illustrating a method of treating the wafer surface according to one preferred embodiment of this invention.

[0021] Referring to Fig. 2A, a wafer 210 is provided. The wafer 210 includes a passivation layer 214 and a plurality of bonding pads 216 on a surface 212. The bonding pads 216 are exposed through openings 218 of the passivation layer 214. The material of the passivation layer 214 can

be inorganic, for example, silicon nitride, silicon oxide or phospho-silicate glass, or organic, for example, polyimide.

[0022] Referring to Figs. 2B-2D, a metal layer 230 and a plurality of solder paste globs 250 are formed on the wafer 210, by those technologies available in this field. The following steps are merely exemplary, and should not be used to limit the scopes of the present invention. The metal layer 230 is a composite layer including an adhesion layer, a barrier layer, and a wetting (solder) layer (not shown), formed by either sputtering or evaporation. The material of the metal layer 230 includes titanium, tungsten, chromium, nickel, copper and the alloys thereof.

[0023] After forming the metal layer 230 on the surface 212 of the wafer 210, a plurality of bumps (solder paste globs) are formed on the bonding pads 226 by either electroplating or screen printing. Taking electroplating as an example, a patterned photoresist layer (not shown) with openings 242 (not shown) is formed on the metal layer 230. Afterwards, solder paste is filled to the openings to form a plurality of solder paste globs 250 by electroplating. The location of each solder paste glob 250 (opening) corresponds to the location of each bonding pad 216. The

material of the solder paste glob can be Pb/Sn alloys, lead-free solder or gold.

[0024] As shown in Fig. 2C, after removing the photoresist layer, a portion of metal layer 230 between the solder paste globs 250 is exposed. Referring to Fig. 2D, using the solder paste globs 250 as an etching mask, a first wet etching process is performed to removed the exposed metal layer 230 between the solder paste globs 250, thus forming an under bump metallurgy (UBM) layer 232. Next, a reflow step is performed to turn the solder paste globs 250 to globular bumps 252, as shown in Fig. 2E. The UBM layer 232 can enhance adhesion between the bumps 252 and the bonding pads 216.

[0025] Similarly, if some photoresist is remained on the metal layer 230 between the solder paste globs 250, the remained photoresist covers the underlying portion of the metal layer 230 in the first wet etching process, leading to residual metal 236 on the passivation layer 214 between the globs 250. The residual metal can deteriorate the yield of the wafer.

[0026] To solve this problem, after the reflow step, a photosensitive material layer 240, for example, a photoresist layer, is formed over the wafer surface 212, partially cov-

ering the bumps 252 and completely covering the underlying UBM layer 232, as shown in Fig. 2F. Referring to Fig. 2G, using the bumps 252 as masks, the photo-sensitive material layer 240 is exposed and developed, thus forming a patterned photo-sensitive material layer 240a. The patterned photo-sensitive material layer 240a is remained under the bumps 252 and covers the UBM layer 232, while the patterned photo-sensitive material layer 240a exposes the passivation layer 214 between the bumps 252. Using the bumps as the mask, the photo-sensitive material layer is patterned in a self-aligned way (i.e. without using a photo-mask), because a certain portion of the photo-sensitive material layer under the bumps is not exposed to light and is not dissolved in the developer.

[0027] Referring to Figs. 2H-2I, a second wet etching process is performed to remove the residues on the wafer surface, including the residual metal 236 between the bumps. The etchant can be etching agent for the UBM layer 232, for example, sulfuric acid or hydrofluoric acid. Because the UBM layer 232 is protected by the patterned photo-sensitive material layer 240a, no undercut will occur to the UBM layer 232. Therefore, the residues on the wafer surface are removed by the second wet etching process

without over-etching or undercut. As a result, the yield is greatly increased. Then, as shown in Fig. 2I, the patterned photo-sensitive material layer 240a is removed by using an organic solvent or an inorganic solvent.

[0028] In addition, a flux (not shown) can be further applied to surfaces of bumps 252 to remove oxides or residues by a reflow step, and the flux is later removed by a solvent. Alternatively, the flux can be applied after the wafer is scribed into chips. In general, the flux can remove oxides on the surface of the bumps and help increase reliability of connection between the chip and the package substrate.

[0029] In conclusion, the method for treating the wafer surface in the present invention can efficiently remove residues on the wafer surface. Using the bumps as the mask, the photo-sensitive material layer is patterned in a self-aligned way, because a certain portion of the photo-sensitive material layer under the bumps is not exposed to the light and is not dissolved in the developer. Since the patterned photo-sensitive material layer completely covers the UBM layer, the second wet etching process can effectively remove residues without damaging the UBM layer. The yield of the bumping process is increased with-

out residues or residual metal on the surface.

[0030] It will be apparent to those skilled in the art that various modifications and variations can be made to the structure of the present invention without departing from the scope or spirit of the invention. In view of the foregoing, it is intended that the present invention cover modifications and variations of this invention provided they fall within the scope of the following claims and their equivalents.